P-Channel Enhancement Mode Field Effect Transistor

- **Features**

V_{DS} (V) = -20V,

I_D = -2A（V_{GS}= -4.5V）

$R_{DS(ON)}$<120mΩ @ V_{GS}= -4.5V

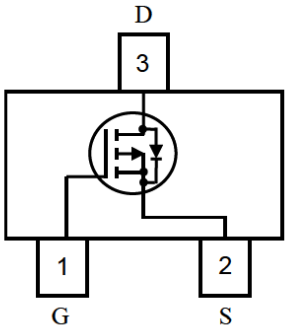
$R_{DS(ON)}$<150mΩ @ V_{GS}= -2.5V

SOT23 Package

- **General Description**

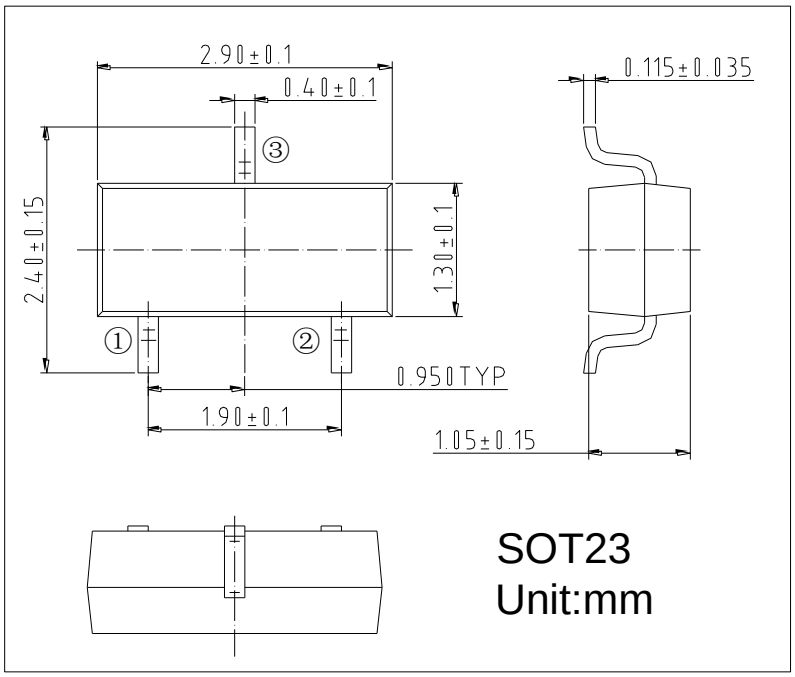
These P-Channel enhancement mode field effect transistors are produced using high cell density, DMOS technology.

- **Pin Configurations**



MARKING:A1SHB

- **Package Information**



- **Absolute Maximum Ratings** @T_A=25℃ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Drain Current (Continuous)	T_A=25°C	I_D	-2	A

	T_A=70°C		-1.8	
Drain Current (Pulse)		I_{DM}	-7	A
Power Dissipation	T_A=25°C	P_D	1	W
Operating Temperature/ Storage Temperature		T_J/T_{STG}	-55~150	℃

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ON/OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D= -250μA	-20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20 V , V_{GS} = 0V	--	--	-1	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} =V_{DS} , I_{DS}=-250μA	-0.4	-0.65	-0.9	V
Gate Leakage Current	I_{GSS}	V_{GS}=±12V , V_{DS}=0V	--	--	±100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$	V_{GS} = -4.5V , I_D= -2A	--	88	120	mΩ
		V_{GS} = -2.5V , I_D= -1A	--	120	150	mΩ
Forward Transconductance	g_{FS}	V_{DS}= -5V , I_D= -2.8A	--	6.5	--	S
Diode Forward Voltage	V_{SD}	I_{SD}= -1.6A , V_{GS}= 0V	--	-0.86	-1.1	V
Max Diode Forward Voltage	I_S		--	--	-1.6	A
Switching CHARACTERISTICS						
Total Gate Charge	Q_g	V_{DS} = -6V, I_D = -2.8A V_{GS} = -4.5V	--	4.9	--	nC
Gate-Source Charge	Q_{gs}		--	0.62	--	nC
Gate-Drain Charge	Q_{gd}		--	1.07	--	nC
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -6V, RL=6Ω I_D = -1A, V_{GEN} = -4.5V R_G = 6Ω	--	10.1	--	ns
Turn-on Rise Time	t_r		--	4.76	--	ns
Turn-off Delay Time	$t_{d(off)}$		--	84.1	--	ns
Turn-off Fall Time	t_f		--	25.2	--	ns
Dynamic CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}= -6V,f= 1.0MHz	--	472	--	pF
Output Capacitance	C_{oss}		--	71	--	pF
Reverse Transfer Capacitance	C_{rss}		--	51	--	pF

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test: PW≤300μ s, duty cycle≤2%.
3. For design AID only, not subject to production testing.
4. Switching time is essentially independent of operating temperature.

Typical Performance Characteristics

Fig.1 Output Characteristic

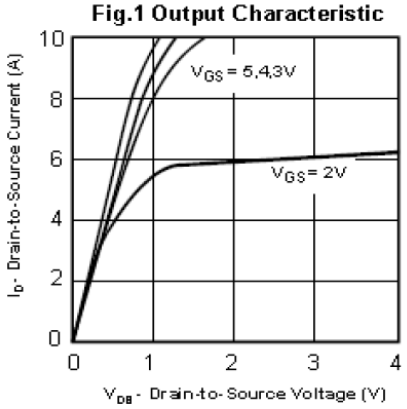


Fig.2 Transfer Characteristics

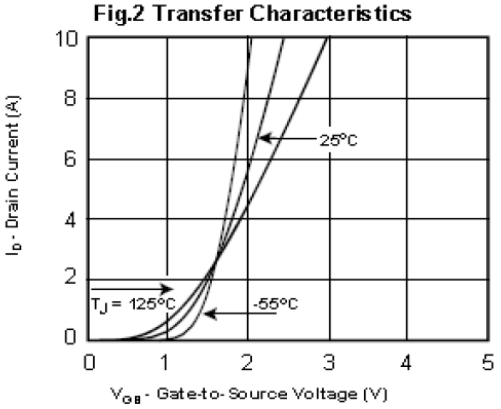


Fig.3 On-Resistance Variation with Temperature

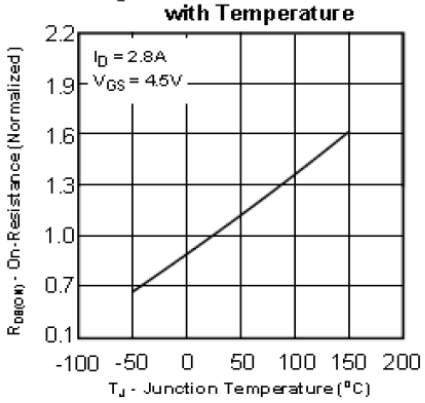


Fig.4 Body Diode Forward Voltage Variation with Source Current

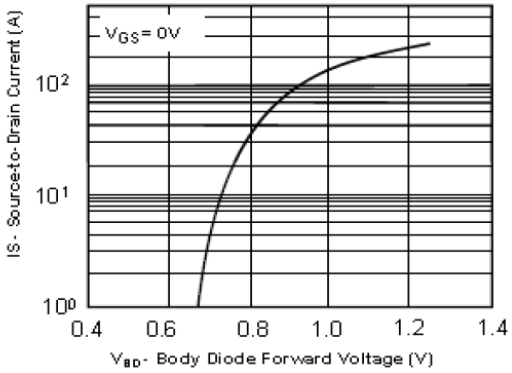


Fig.5 Gate Threshold Variation with Temperature

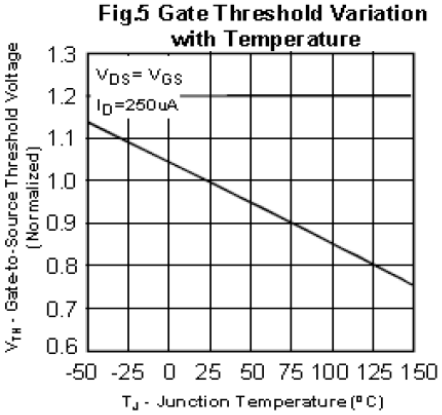


Fig.6 Capacitance

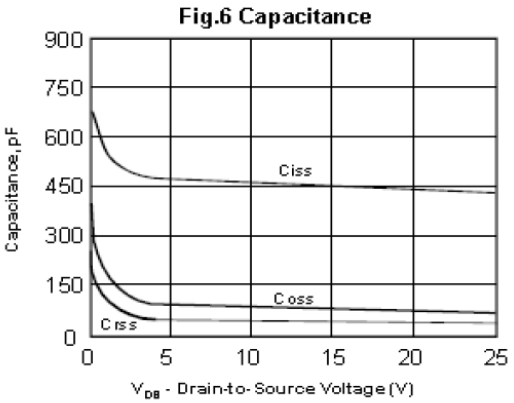


Fig. 7 Gate Charge Waveform

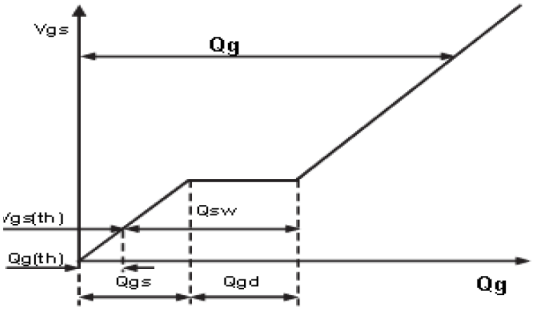


Fig. 8 Gate Charge

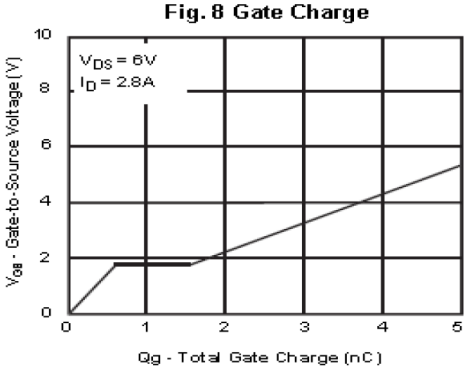


Fig. 9 Maximum Safe Operating Area

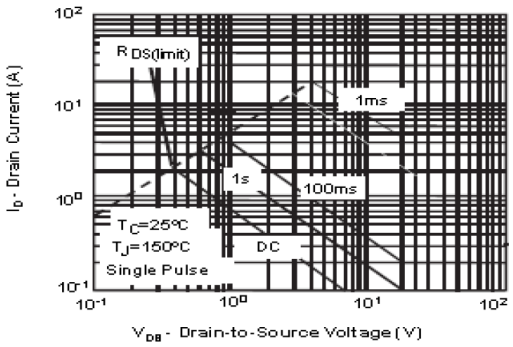


Fig. 10 Normalized Thermal Transient Impedance Curve