P-Channel Enhancement Mode Field Effect Transistor

- **Features**

V_{DS}(V) = -22V, I_D = -2.2A

$R_{DS(on)}$ = 100mΩ @V_{GS} = -4.5V

$R_{DS(on)}$ = 120mΩ @V_{GS} = -2.5V

High density Cell Design for Low $R_{DS(ON)}$

Voltage controlled small signal switch

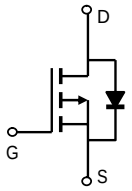
Reliable and Rugged

- **General Description**

These P-Channel enhancement mode field effect transistors are produced using high cell density, DMOS technology.

- **Pin configurations**

See Diagram below



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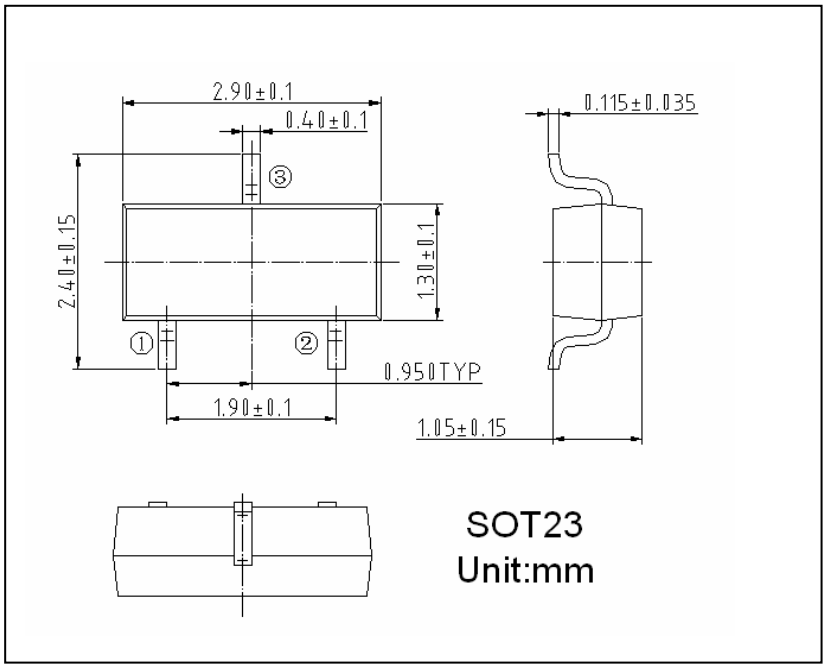
- **Package Information**



- **Absolute Maximum Ratings** @T_A=25℃ unless otherwise noted

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DSS}	-22	V
Gate-Source Voltage	V_{GSS}	±8	V
Drain Current (Continuous)	I_D	-2.2	A
Drain Current (Pulse)	I_{DM}	-10	A
Power Dissipation	P_D	350	mW
Operating Temperature/ Storage Temperature	T_J/T_{STG}	-55~150	℃

- **Electrical Characteristics** @T_A=25℃ unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D=-250uA	-22	--	--	V
Drain Cut-off Current	I_{DSS}	V_{DS} = -20 V , V_{GS} = 0V	--	--	-1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS} =±8 V , V_{DS} = 0V	--	--	±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	I_D = -250 uA , V_{DS} = V_{GS}	-0.45	-0.75	-1.5	V
Drain-Source On-state Resistance	$R_{DS(ON)}$	V_{GS} = -4.5V ,I_D =-2.8 A	--	100	130	mΩ
		V_{GS} = -2.5V , I_D = -2A	--	120	200	mΩ
Forward Transconductance	G_{FS}	V_{DS} = -5V, I_D = -2.8A	--	6.5	--	S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = -6V , V_{GS} = 0V F = 1 MHz	--	415	--	pF
Output Capacitance	C_{OSS}		--	223	--	pF
Feedback Capacitance	C_{RSS}		--	87	--	pF
SWITCHING CHARACTERISTICS						
Turn-on Delay Time	$T_{D(ON)}$	V_{DD} = -6V , R_L = 6Ω , I_D = -1.0A,	--	13	25	ns
Turn-off Delay Time	$T_{D(OFF)}$	V_{GEN} = -4.5V, R_G = 6Ω	--	42	70	ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	Is = -1.6A, V_{GS} = 0V	-0.5	--	-1.2	V

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test: PW≤300μs, duty cycle≤2%.
3. For design AID only, not subject to production testing.
4. Switching time is essentially independent of operating temperature.

- **Typical Performance Characteristics**

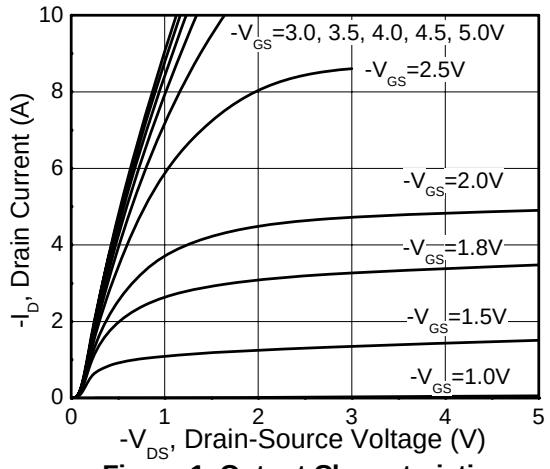


Figure 1. Output Characteristics

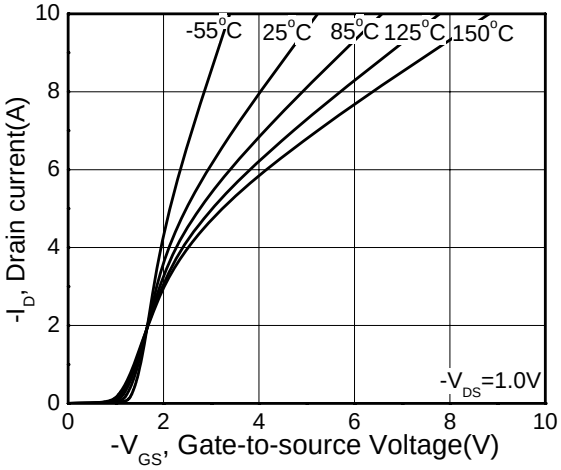


Figure 2. Transfer Characteristics

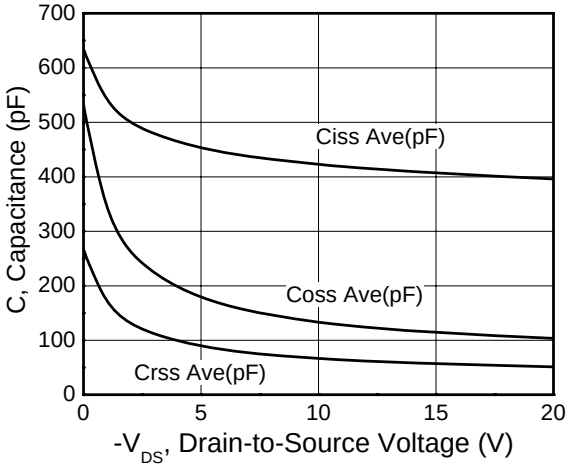


Figure 3. Capacitance

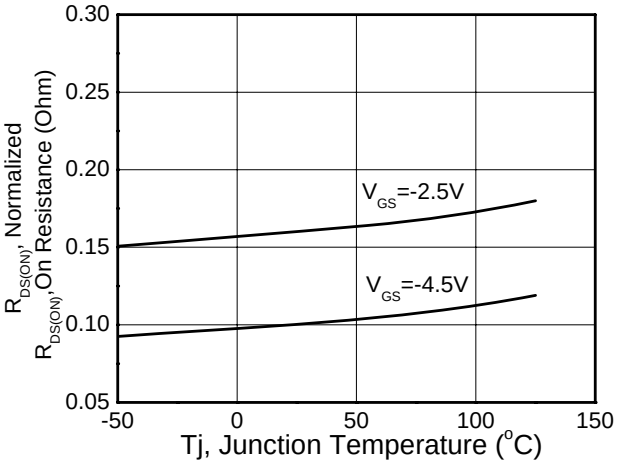


Figure 4. On Resistance Vs. Temperature

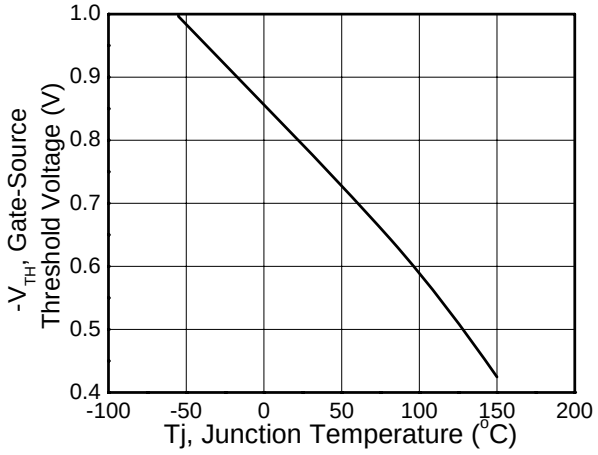


Figure 5. Gate Thershold Vs. Temperature

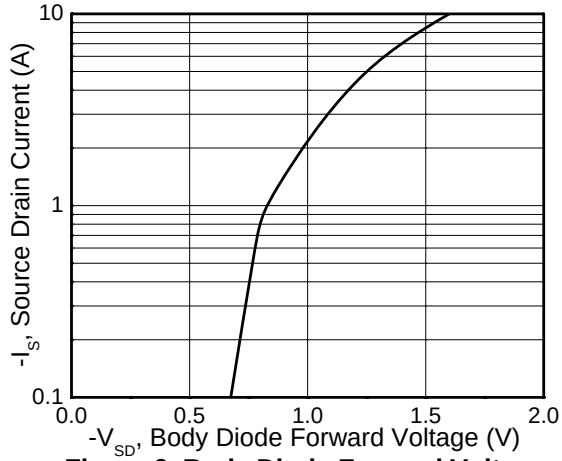


Figure 6. Body Diode Forward Voltage Vs. Source Current